

ABSTRACT OF THE DISCLOSURE

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A synchronous read channel having a single chip integrated circuit digital portion which provides digital gain control, timing recovery, equalization, digital peak detection, sequence detection, RLL(1,7) encoding and decoding, error-tolerant synchronization and channel quality measurement is disclosed. The integrated circuit accommodates both center sampling and side sampling, and has a high degree of programmability of various pulse shaping and recovery parameters and the ability to provide decoded data using sequence detection or digital peak detection. These characteristics, together with the error-tolerant sync mark detection and the ability to recover data when the sync mark is obliterated, allow a wide variety of retry and recovery strategies to maximize the possibility of data recovery. Various embodiments, including an embodiment incorporating the analog functions as well as the primary digital functions of the read channel in a single integrated circuit, and preferred embodiments utilizing a reduced complexity, programmable modified Viterbi detector supporting a broad class of partial response channels are disclosed.